CLAIMS

1. An apparatus comprising:

a circuit configured to translate instruction codes of a first instruction set into sequences of instruction codes of a second instruction set that emulate a functionality of the instruction codes of the first instruction set.

2. The apparatus according to claim 1, wherein said sequences of instruction codes of a second instruction set are stored in a computer readable medium.

3. The apparatus according to claim 2, wherein said computer readable medium comprises a microcode memory.

4. The apparatus according to claim 3, wherein said instruction codes of said first instruction set are used to address said microcode memory.

5. The apparatus according to claim 3, wherein addresses into said microcode memory are generated by a look-up-

table in response to said instruction codes of said first instruction set.

6. The apparatus according to claim 1, wherein said instruction codes of said second instruction set comprise native instructions of a target processor.

7. The apparatus according to claim 6, wherein said target processor is selected from the group consisting of MIPS, ARM, and Motorola 68K.

8. The apparatus according to claim 3, wherein said microcode memory can be reprogrammed to support different processors.

9. The apparatus according to claim 1, wherein said circuit is configured to format the sequences of instruction codes of said second instruction set according to an opcode format of a processor.

10. The apparatus according to claim 1, wherein said circuit is configured to detect optimizable sequences of instruction codes on-the-fly.

11. The apparatus according to claim 1, wherein said circuit comprises a sequence optimization circuit.

12. The apparatus according to claim 1, wherein said circuit comprises a native instruction sequence generator circuit.

13. The apparatus according to claim 1, wherein said circuit is coupled between a processor and a memory system.

14. The apparatus according to claim 13, wherein said circuit is configured to (i) directly connect said processor and said memory system during a first state of operation and (ii) during a second state of operation, communicate with said processor as though said circuit was the memory system and communicate with said memory system as though said circuit was the processor.

15. The apparatus according to claim 1, wherein said instruction codes of said first instruction set comprise Java bytecodes.

16. The apparatus according to claim 1, wherein said circuit comprises a hardware portion of a Java virtual machine.

17. An apparatus comprising:

means for translating instruction codes of a first instruction set into sequences of instruction codes of a second instruction set;

means for receiving said instructions of said first instruction set; and

means for presenting said instructions of said second instruction set.

18. A method for on-the-fly translation of instructions of a first instruction set into instructions of a second instruction set comprising the steps of:

(A) receiving an instruction code of said first instruction set;

(B) generating a sequence of instruction codes of said second instruction set that will emulate said instruction code of said first instruction set using a hardware translator; and

(C) presenting said sequence of instruction codes of said second instruction set.

19. The method according to claim 18, wherein step C comprises the sub-step of:

(C-1) selecting said sequence of instruction codes of said second instruction set from a microcode memory in response to said instruction codes of said first instruction set.

20. The method according to claim 19, wherein step C further comprises the sub-step of:

(C-2) optimizing said sequence of instruction codes of said second instruction set for a particular processor.